ABSTRACT OF THE DISCLOSURE

A serial-to-parallel converter circuit is constructed of a plurality of D flip-flops receiving, as a clock signal, data in a single signal of serial data stored in a ROM. Each D flip-flop transmits "high" data to a next stage through a latch operation every time a piece of the data is read from the ROM. The plurality of D flip-flops converts the signal of serial data to parallel data by producing output signals as control signals. According to this arrangement, a signal production circuit and a display device incorporating it become available which allow for a reduction in the capacity, cost, and dimensions of the storage means, and also in the wiring and substrate areas required around the storage means, through more efficient use of the data stored in the storage means.